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jc857 U.S. PTO 02/19/02

UTILITY PATENT APPLICATION TRANSMITTAL For non-provisional application under 37 CFR 1 53(b)	Attorney Docket: **D900D/1368D** Lead Inventor: **Marina V. PLAT and Angela T. HUI** Title: **METHOD AND SYSTEM FOR REDUCING ARC LAYER REMOVAL DURING REMOVAL OF PHOTORESIST** **Express Mail No.: EL815320820US**

APPLICATION ELEMENTS	Address to: **Assistant Commissioner for PATENTS Box Patent Applications Washington, D.C. 20231**
1. [X] Fee Transmittal Form PTO/SB/17	**ACCOMPANYING APPLICATION PARTS**
2. [X] Specification: Fifteen (15) pages; [X] Claims: Three (3) pages; [X] Abstract: One (1) page	7. [ ] Assignment and Recordation Cover 8. [ ] Statement by Assignee (37 CFR 3.73(b) [X] Power of Attorney (copy)
3. [X] Drawings: Seven (7) sheets;	9. [ ] English Translation (*if applicable*)
4. [X] Declaration by Inventors: Two (2) pages; a. [ ] Newly executed (original or copy) b. [X] Copy from Prior Application: 37 CFR 1.63(d)(2) (for Continuation/Divisional: Box 16 completed below) i. [ ] Deletion of Inventor(s) Signed statement attached deleting inventor(s) named in Prior Application – 37 CFR 1 63(d)(2) and 1 33(b)	10. [ ] Information Disclosure Statement [ ] PTO Form 1449 [ ] References 11. [X] Preliminary Amendment 12. [X] Return Receipt Postcard (*itemized*)
5. [ ] Microfiche Computer Program (*Appendix*)	13. [ ] Small Entity Status Declaration [ ] Statement filed in Prior Application, status still proper and desired
6. [ ] Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all necessary*) a. [ ] Computer Readable Copy b. [ ] Paper Copy (identical to computer copy) c. [ ] Statement verifying identity of above copies	14. [ ] Certified Copy of Priority Document(s) 15. Other: _____

j1002 U.S. PTO 10/079775 02/19/02

16. **Continuing Application** (*check appropriate box and supply requisite information below and in a Preliminary Amendment*) :

[ ] Continuation [X] Divisional [ ] Continuation-in-Part (CIP) of Prior Application No: **09/433,541**

Prior Application information: Examiner: Warren, M. Group Art Unit: 2815 Filing Date: November 2, 1999

For CONTINUATION or DIVISIONAL application only: *The entire disclosure of the prior application, from which an Oath or Declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.*

17. **CORRESPONDENCE ADDRESS**

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Attorney for Applicant

February 19, 2002
Date

PTO/SB/17 (2/98)
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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.

These are the fees effective October 1, 1999

Small Entity payments must be supported by a Small Entity Statement, otherwise, large entity fees must be paid. See Forms PCT/SB/m9-12 See 37 CFR 1 27 and 1 28.

Serial No.:	**To Be Assigned**
Filing Date:	**Herewith**
Inventor:	**Marina V. PLAT and Angela T. HUI**
Examiner:	**To Be Assigned**
Group Art Unit:	**To Be Assigned**
Attorney Docket:	**D900D/1368D**

TOTAL AMOUNT OF PAYMENT **$740.00**

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge all fees and credit any overpayment associated with this communication to:

Deposit Account No: 01-0365

Name: **Advanced Micro Devices, Inc.**

[X] Charge any additional fees required under 37 CFR 1 16 and 1 17

2. [ ] Payment Enclosed:

[ ] Check No. * [ ] Money Order [ ] Other

FEE CALCULATION

1. Basic Filing Fee:

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Description	Fee Paid
101	740.00	201	370 00	Utility filing fee	$740 00
106	330.00	206	165 00	Design filing fee	______
107	510.00	207	255.00	Plant filing fee	______
108	740 00	208	370 00	Reissue filing fee	______
114	160 00	214	80 00	Provisional filing	______

SUBTOTAL (1) $740.00

2. EXTRA CLAIMS FEES

Total Claims	Extra Claims	Fee	Fee Paid
7 - 20 =	*	x 18 =	$ 0.00
Independent Claims			
2 - 3 =	*	x 84 =	$ 0.00

SUBTOTAL (2) $ 0.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

FEE DESCRIPTION	Fee Paid
Surcharge late filing of fee or oath	
Surcharge late provisional filing fee or cover sheet	
Non-English specification	
For filing a request for reexamination	
Requesting publication or SIR prior to Examiner Action	
Extension for reply within first month	
Extension for reply within second month	
Extension for reply within third month	
Extension for reply within fourth month	
Extension for reply within fifth month	
Notice of Appeal	
Filing a brief in support of an appeal	
Request for oral hearing	
Petition to institute a public use proceeding	
Petition to revive - unavoidable	
Petition to revive - unintentional	
Utility issue fee (or reissue)	
Design issue fee	
Plant issue fee	
Petitions to the Commissioner	
Petitions related to provisional applications	
Submissions of Information Disclosure Statement	
Recording of each patent assignment per property (times number of properties)	
Filing submission after final rejection (37 CFR 1.129(a))	
For each additional invention to be examined (37 CFR 1.129(b))	
Other fee (specify): ______	
Other fee (specify): ______	

SUBMITTED BY

Joseph A. Sawyer, Jr., Reg. No., 30,801
Attorney for Applicant

February 19, 2002
Date

EXPRESS MAIL CERTIFICATE

I hereby certify that the above paper/fee is being deposited with the Unites States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231, on **February 19, 2002**. Express Mail No.: **EL815320820US**. Signature of Person mailing paper/fee:

Grace Alicea

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Date: February 19, 2002

Marina V. PLAT and Angela T. HUI

Serial No.: To Be Assigned Group Art Unit: To Be Assigned

Filed: Herewith Examiner: To Be Assigned

For: METHOD AND SYSTEM FOR REDUCING ARC LAYER REMOVAL DURING REMOVAL OF PHOTORESIST

Box: Patent Application
Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please enter the following amendments and remarks into the above-identified patent application.

IN THE SPECIFICATION

Before "**FIELD OF THE INVENTION**," please insert:

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a divisional of USSN 09/433,541, filed November 2, 1999, and assigned of record to Advanced Micro Devices, Inc., of Sunnyvale, California.

IN THE CLAIMS

Please cancel claims 7-12.

REMARKS

The present application is a divisional of United States Patent Application Serial Number 09/433,541, filed November 2, 1999. This Preliminary Amendment is submitted to more particularly claim the present invention. Claims 1-12 are pending in the present application. Claims 7-12 are canceled. Claims 1-6 remain pending.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

February 19, 2002
Date

Joseph A. Sawyer, Jr.
Attorney for Applicant
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Before "**FIELD OF THE INVENTION**," please insert:

--CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a divisional of USSN 09/433,541, filed November 2, 1999, and assigned of record to Advanced Micro Devices, Inc., of Sunnyvale, California.--

METHOD AND SYSTEM FOR REDUCING ARC LAYER REMOVAL DURING REMOVAL OF PHOTORESIST

FIELD OF THE INVENTION

The present invention relates to semiconductor devices, such as flash memory devices, more particularly to a method and system for reducing removal of the antireflective-coating layer during removal of the photoresist layer.

BACKGROUND OF THE INVENTION

A conventional semiconductor device, such as a conventional embedded flash memory, includes a large number of memory cells in a memory region. The memory cells are typically floating gate devices, such as floating gate transistors. The conventional embedded memory may also include logic devices in a second region, or core, of the conventional embedded memory. The logic and memory regions of the conventional embedded memory are typically processed separately.

Figure 1 is a flow chart depicting a conventional method 10 for processing a portion of a conventional semiconductor device, such as a conventional embedded flash memory. A polysilicon layer is deposited across a semiconductor substrate, via step 12. The polysilicon layer is typically deposited on a thin insulating layer grown on the substrate. A conventional SiON antireflective coating ("ARC") layer of a desired thickness is then deposited, via step 14. The conventional ARC layer must be deposited in a very narrow range of the desired thickness in step 14. This is because the antireflective properties of the conventional ARC layer are highly dependent upon the thickness of the conventional ARC layer. Typically, the desired thickness of the conventional ARC layer is three hundred Angstroms plus or minus

ten percent (thirty Angstroms).

A first photoresist layer is then patterned on the conventional ARC layer, via step 16. The first photoresist layer pattern is typically obtained by spinning a layer of photoresist onto the ARC layer and exposing portions of the photoresist layer to light through a mask layer to develop a pattern, or mask, in the photoresist layer. The first photoresist layer patterned in step 16 typically completely covers the logic region of the conventional imbedded memory. The first photoresist layer also includes a pattern over the memory region to define stacked gates in the memory region of the conventional imbedded memory.

Once the first photoresist pattern has been defined, the stacked gates of the memory region are etched, via step 18. The first resist layer is then removed and residues cleaned using a wet etch, via step 20. A second photoresist pattern is then defined, via step 22. Step 22 typically includes spinning a second layer of photoresist onto the conventional embedded memory and developing the pattern of the second photoresist structure using conventional photolithography. Masking in the second photoresist layer defines gates in the logic region of the conventional imbedded memory, while the second photoresist layer also covers the memory region to ensure that processing of the logic region does not affect the memory region. The gates in the logic region are then etched, via step 24. The second photoresist layer may then be stripped and residues cleaned, via step 26. Processing of the conventional imbedded memory is then completed, via step 28.

Although the conventional method 10 can be used, one of ordinary skill in the art will readily understand that the conventional method 10 results variations in the critical dimension of structures fabricated in the logic region of the conventional embedded memory. When photoresist is spun onto the conventional embedded memory in steps 16 or

22, the photoresist will vary in thickness. This is particularly true when the topology of the layers under the photoresist is not flat.

Variations in the photoresist layer thickness cause variations in the critical dimension of structures desired to be formed, otherwise known as the swing curve effect. Figure 2 is a graph 30 depicting the swing curve effect, variations in critical dimension versus photoresist thickness. The plot 31 indicates the desired size, or desired critical dimension, of a particular feature. The desired size is set by the design of the conventional embedded memory and thus is independent of resist thickness. The plot 32 depicts the variation in critical dimension versus photoresist thickness when a conventional ARC layer of the appropriate thickness is used. Because the conventional ARC layer of the appropriate thickness is used, reflections from the layer(s) underlying the photoresist layer are reduced. Thus, the structures formed using the photoresist layer have a critical dimension that is close to the desired critical dimension.

Curve 34 depicts the variation in the critical dimension for the structure of the desired size when no conventional ARC layer or a conventional ARC layer of an incorrect thickness is used. The antireflective properties of the ARC layer are highly dependent on thickness of the ARC layer. When a resist pattern is formed without the ARC layer, light used in conventional photolithography may reflect off of the layer(s) and structures under the photoresist layer. The reflected light causes variations in critical dimensions of structures etched in the polysilicon layer and causes a phenomenon called reflective notching, a narrowing of the polysilicon lines as a result of reflections from the underlayer. Thus, the critical dimensions of structures fabricated with no conventional ARC layer or a conventional ARC layer without the desired thickness vary more strongly with photoresist

thickness. This variation is shown in curve 34.

Figure 3A depicts a portion of a conventional embedded memory 40 after step 16, patterning the first resist layer, is performed. The conventional embedded memory 40 includes a logic region 44 and a memory region 42. A polysilicon layer 51 is provided on substrate 50. Note that an insulating layer (not shown) typically separates the polysilicon layer 51 from the substrate 50. In addition, underlying structures 47 and 49 are shown. Structures 47 and 49 were obtained prior to deposition of the polysilicon layer 51. A conventional ARC layer 52 having the desired thickness for reducing reflections is provided on the polysilicon layer 51. The thickness of the conventional ARC layer 52 is typically three hundred Angstroms plus or minus approximately ten percent. The first photoresist structure 53 covers the logic region 44, but defines the pattern for stacked gates in the memory region 42. Note that the first photoresist structure 53 varies in thickness.

Figure 3B depicts a portion of a conventional embedded memory 40 after step 18, etching gates in the memory region 42, of the method 10 shown in Figure 1 is performed. Referring to Figure 3B, stacked gates 54, 56 and 58 have been formed in the memory region 42 of the conventional embedded memory 40. The stacked gates 54, 56 and 58 are covered by remaining portions 55, 57 and 59, respectively, of the ARC layer 52. Portions of the first photoresist layer 53 still covers the stacked gates 54, 56 and 58 as well as the polysilicon layer 51 and the conventional ARC layer 52 in the logic region 44. Because the conventional ARC layer 52 has the desired thickness, the critical dimensions of gates 54, 56 and 58 are quite close to what is desired. In other words, variations in the critical dimension of the gates 54, 56 and 58 may follow the curve 32 depicted in Figure 2.

Figure 3C depicts a portion of a conventional embedded memory 40 after step 20,

stripping the first photoresist structure 53, of the method 10 shown in Figure 1 is performed. Referring to Figure 3C, a portion of the conventional ARC layer 52 has been removed during the strip of the photoresist structure 53. Thus, the conventional ARC layer 52 is thinner than in Figure 3B. Typically, twenty to fifty Angstroms are removed during the wet resist strip after the etch performed in step 20. After the etch, the thickness of the conventional ARC layer 52 is twenty to fifty Angstroms thinner than the optimal thickness. Consequently, removal of a portion of the conventional ARC layer 52 during the resist strip is likely to significantly reduce the ability of the conventional ARC layer 52 to decrease reflections. Thus, the gates formed in step 24 in the logic region 44 will have critical dimensions which vary greatly. In other words, the critical dimensions of structures, such as gates, in the logic region will follow the curve 44 shown in Figure 2. These large variations are undesirable. In order to reduce these variations in the logic region 44, the ARC layer 52 and photoresist structure 53 would be removed. The ARC layer 52 would then be replaced with another ARC layer (not shown) that is deposited at the desired thickness.

Accordingly, what is needed is a system and method for providing the conventional semiconductor device, such as an imbedded memory, in which the ARC layer need not be removed and redeposited. The present invention addresses such a need.

SUMMARY OF THE INVENTION

The present invention provides a method and system for providing a semiconductor device. The semiconductor device includes a first layer to be etched. The method and system comprise depositing an antireflective coating (ARC). The method and system also comprise patterning a resist layer, the resist layer has a pattern including a plurality of apertures

therein. The resist layer is for etching the first layer. A first portion of the first layer and a second portion of the ARC layer are exposed by the pattern. The method and system also comprise etching the first portion of the first layer and the second portion of the ARC layer and removing the resist layer utilizing a plasma etch. The ARC layer is resistant to the plasma etch.

According to the system and method disclosed herein, the present invention reduces the removal of the ARC layer by using a plasma etch to strip photoresist. The ARC layer is resistant to removal by the plasma etch. Consequently, the ARC properties of the ARC layer are preserved, allowing a reduction in the swing curve effect and reflective notching.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a flow chart of a conventional method for providing a portion of semiconductor device

Figure 2 is a graph depicting the variation in critical dimension versus photoresist thickness.

Figure 3A is diagram of a portion of a conventional embedded memory after the first photoresist layer has been patterned.

Figure 3B is a diagram of a portion of the conventional embedded memory after the stacked gates have been etched.

Figure 3C is a diagram of a portion of the conventional embedded memory after the first photoresist layer has been removed and residues cleaned.

Figure 4A is a flow chart depicting one embodiment of a method for providing a portion of a semiconductor device and an ARC layer in accordance with the present

invention.

Figure 4B is a more detailed flow chart depicting one embodiment of a method for providing a portion of a semiconductor device in accordance with the present invention.

Figure 5A is a diagram depicting one embodiment of a semiconductor device in accordance with the present invention after the first photoresist structure has been provided.

Figure 5B is a diagram depicting one embodiment of a semiconductor device in accordance with the present invention after the first photoresist structure has been stripped.

Figure 5C is a diagram depicting one embodiment of a semiconductor device in accordance with the present invention after the second photoresist structure has been stripped.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to an improvement in semiconductor processing. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be applied to other embodiments. Thus, the present invention is not intended to be limited to the embodiment shown, but is to be accorded the widest scope consistent with the principles and features described herein.

Conventional semiconductor devices are typically processed using conventional antireflective coating (ARC) layers. For example, a conventional semiconductor device, such as an embedded flash memory, contains a logic region and a memory region. In order to pattern gates with a narrow distribution of the critical dimension in the logic region and the

memory region, a conventional ARC layer is deposited on a polysilicon layer. The conventional ARC layer is typically SiON. The antireflective properties of the conventional ARC layer are highly dependent on the thickness of the conventional ARC layer. Typically, the conventional ARC layer has a desired thickness of three hundred Angstroms plus or minus approximately thirty Angstroms thick. Outside of the desired thickness, the conventional ARC layer may not adequately reduce or prevent reflections.

Typically, the conventional ARC layer is deposited with the desired thickness. The gates in the memory portion of the conventional imbedded memory are then patterned. Typically, this includes patterning a first layer of photoresist and etching the polysilicon and conventional ARC layer. The first layer of photoresist completely covers the logic region of the conventional memory and is patterned in the memory region. After the stacked gates are etched, the first photoresist layer is stripped using a wet chemical. The gates in the logic portion of the conventional imbedded memory are then patterned. This step is typically performed by patterning a second photoresist layer and etching the polysilicon and conventional ARC layer under apertures in the second photoresist layer. For this step, the second photoresist layer typically covers the memory region and is patterned in the logic region of the conventional imbedded memory. Thus, the gates in the memory region and the gates in the logic region are processed independently.

The stripping of the photoresist structure after gates in the memory region are formed using the first etch removes a significant portion of the conventional ARC layer, typically twenty to fifty Angstroms. The desired thickness of the conventional ARC layer is approximately three hundred Angstroms plus or minus about ten percent. Thus, removal of a portion of the conventional ARC layer during the photoresist strip may take the conventional

ARC layer far enough away from the desired thickness that the conventional ARC layer is no longer efficient. Thus, when the structures, such as gates, in the logic region are formed, the critical dimension of the structures varies greatly due to the swing curve effect and reflective notching.

One method for remedying this would be to deposit a thicker conventional ARC layer at the outset. Once the first photoresist structure is stripped, the conventional ARC layer would have the desired thickness. Variations of the critical dimensions of structures in the logic region due to the swing curve effect would be reduced. However, because the conventional ARC layer was thicker as provided, the conventional ARC layer might not function properly for processing of the memory region. Thus, variations in the critical dimensions of structures in the memory region due to the swing curve effect or reflective notching would be greatly increased.

The present invention provides a method and system for providing a semiconductor device. The semiconductor device includes a first layer to be etched. The method and system comprise depositing an antireflective coating (ARC). The method and system also comprise patterning a resist layer. The resist layer has a pattern including a plurality of apertures therein. The resist layer is for etching the first layer. A first portion of the first layer and a second portion of the ARC layer are exposed by the pattern. The method and system also comprise etching the first portion of the first layer and the second portion of the ARC layer and removing the resist layer utilizing a plasma etch. The ARC layer is resistant to the plasma etch.

The present invention will be described in terms of a particular device having certain components and particular techniques for performing certain steps, such as the use of a

particular capping layer having a certain thickness. However, one of ordinary skill in the art will readily recognize that this method and system will operate effectively for other devices having other components and other techniques. Furthermore, the present invention will be described in terms of a particular semiconductor memory device, an embedded memory. However, nothing prevents the method and system from being utilized with another semiconductor device.

To more particularly illustrate the method and system in accordance with the present invention, refer now to Figure 4A, depicting one embodiment of a method 100 in accordance with the present invention for providing a semiconductor device such as an embedded memory. The method 100 preferably commences after a first layer to be etched has been provided. In a preferred embodiment, the method 100 commences after a polysilicon layer desired to be patterned has been deposited. The polysilicon layer is to be patterned into stacked gates and logic gates. An ARC layer of a desired thickness is provided, preferably by depositing the ARC layer, via step 102. Preferably, the ARC layer deposited in step 102 is a SiON layer. Also in a preferred embodiment, the desired thickness of the ARC layer is the thickness desired for maximizing the antireflective properties of the ARC layer. In one embodiment, this thickness is three hundred Angstroms plus or minus ten percent. However, the ARC layer may have another desired thickness. For example, in some other applications, the desired thickness of the ARC layer may be one hundred to five hundred Angstroms. A photoresist layer is then patterned on the ARC layer, via step 104. The photoresist structure includes a pattern which has apertures over the regions desired to be etched and covers regions desired to be preserved. The ARC layer and underlying first layer are then etched, via step 104. Because the ARC layer has the desired thickness, variations in the critical

dimensions of structures etched into the first layer due to variations in the thickness of the photoresist structure are reduced. Thus, gates may be formed in a region of the embedded memory. The photoresist layer is then etched using a plasma etch to which the ARC layer is resistant, via step 108. Thus, the ARC layer is resistant to removal by the plasma etch. In contrast, the photoresist structure is layer by the plasma etch. In other words, the selectivity of the etch for the photoresist is relatively high, while the selectivity of the etch for the ARC layer is relatively low. Consequently, little or none of the ARC layer is removed when the photoresist structure is removed. Because the ARC layer is protected from removal, the antireflective properties of the ARC layer are preserved for later use. As a result, the critical dimensions of the structures formed using the ARC layer after removal of the photoresist structure will not vary greatly due to the swing curve effect.

Figure 4B depicts a more detailed flow chart of a method for providing a portion of a semiconductor device, such as an embedded memory, which has a logic region and a memory region. A polysilicon layer is deposited on a semiconductor substrate, via step 112. The polysilicon layer is analogous to the first layer discussed with respect to Figure 4A. The polysilicon layer is to be patterned into the stacked and logic gates. Referring back to Figure 4B, a SiON ARC layer is deposited at the desired thickness for antireflective properties of the SiON ARC layer, via step 114. In a preferred embodiment, the desired thickness is approximately three hundred Angstroms plus or minus approximately thirty Angstroms. A first resist structure is then patterned, via step 116. Preferably, step 116 includes spin-coating photoresist on the embedded memory and developing a pattern in the photoresist using photolithography. The first resist layer includes a pattern that has apertures over a first region and covers a second region. Thus, the first resist structure is for fabricating structures

in the first region of the embedded memory. In a preferred embodiment, the first resist structure is for providing stacked gates in the memory region of the embedded memory. Thus, in a preferred embodiment, the first region of the embedded memory is the memory region. The structures in the first region are then defined using an etch, via step 118. The first photoresist structure is then stripped using a plasma etch that uses a plasma including a forming gas, via step 120. The plasma used in step 120 thus etches the photoresist. However, the ARC layer is resistant to removal by the plasma used in step 120. Consequently, the photoresist strip performed in step 120 removes little or none of the ARC layer.

An optional wet preclean, for example using sulfuric acid, may then be performed, via step 122. The wet preclean removes any remaining residues from the plasma etch performed in step 122. Although the ARC layer is exposed to the wet etchant in the wet preclean, the preclean is only used to remove residues. Consequently, exposure of the ARC layer to the wet etchant is greatly reduced. Thus, the amount of the ARC layer removed by the wet etchant is still greatly reduced over the amount of the ARC layer removed by a conventional photoresist strip.

A second resist layer for a second portion of the semiconductor device is then patterned, via step 124. Preferably, step 124 includes spin-coating photoresist on the embedded memory and developing a pattern in the photoresist using photolithography. The second resist layer has a pattern including apertures over the second region and covers the first region. Thus, the second resist layer is for fabricating structures in the second region of the embedded memory. In a preferred embodiment, the second resist layer is for providing gates in the logic region of the embedded memory. Thus, in a preferred embodiment, the second region of the embedded memory is the logic region. The structures in the second

region of the semiconductor device are then etched, via step 126. Thus, gates in the logic region may be defined in step 126. Processing of the embedded memory may be completed, via step 128. Step 128 thus includes stripping the second photoresist layer and performing any subsequent processing steps. Step 128 may also include removing the ARC layer prior to formation of subsequent structures.

Because the photoresist is stripped using a plasma etch to which the ARC layer is resistant, the ARC layer is less susceptible to removal by the photoresist strip in accordance with the present invention. In one embodiment, the photoresist strip in accordance with the present invention does not remove any of the ARC layer. In another embodiment, a photoresist strip removes in accordance with the present invention only a small portion of the ARC layer. This portion is small enough to allow the ARC layer to continue to act as an antireflective layer. The preservation of most or all of the ARC layer is in contrast to removal of ten to twenty Angstroms of a conventional ARC layer using a conventional wet photoresist strip. Because the ARC layer is less subject to removal by a photoresist strip in accordance with the present invention, the thickness of the ARC layer is preserved for fabrication of structures in the second portions of a semiconductor device. The ARC layer can thus still reduce the variation of the critical dimensions of structures fabricated. Furthermore, because the ARC layer has the desired thickness as provided, the variations in the critical dimensions of structures fabricated in the first region are also reduced. For example, the stacked gates of the memory region and the gates of the logic region can both be formed without being subject to wide variations in critical dimension due to the swing curve effect. Consequently, processing of a semiconductor device, such as an embedded memory, is facilitated.

For example, refer to Figures 5A-5C, depicting an embedded memory 200 during processing in accordance with the methods 100 or 110. Figure 5A depicts the embedded memory 200 after step 104 or 116 of patterning the first photoresist structure has been performed. The embedded memory 200 includes a memory region 202 and a logic region 204. A polysilicon layer 212 has been deposited on a substrate 210. The polysilicon layer 212 is generally separated from the substrate 210 by a thin insulating layer (not shown). In addition, underlying structure 201 and 203 in the logic and memory regions, respectively, are shown. The ARC layer 214 has been provided on the polysilicon layer 212 at the desired thickness. The photoresist structure 216 has also been provided. The photoresist structure 216 includes apertures exposing the ARC layer 214 and the underlying polysilicon layer 212.

Figure 5B depicts the semiconductor device 200 after the first resist layer has been stripped using a photoresist strip in accordance with the present invention, such as in steps 108 or 120. The stacked gates 220, 222 and 224 have been provided in the memory region 202. Because of the etching, only portions 221, 223 and 225 of the ARC layer 214 remain in the memory region 202. Because the ARC layer was deposited at approximately the desired thickness, the stacked gates 220, 222 and 224 have critical dimensions close to what is desired. Thus, the ARC layer 214 has greatly reduced the swing curve effect in the memory region. No structures have been formed in the logic region 202. Furthermore, the resist strip using the plasma etch has not greatly affected the thickness of the ARC layer 214 because the ARC layer is resistant to removal by the plasma etch. Consequently, the ARC layer 214 still retains sufficient antireflective properties to be used in fabricating structures in the logic region 204.

Figure 5C depicts the semiconductor device 200 after removal of the second resist

structure. Thus, the gates 230, 232 and 234 have been defined in the logic region 204. Because of the presence of the ARC layer 214, remaining as regions 231, 233 and 235, the critical dimensions of structures in the logic region 204 do not vary greatly. Thus, the swing curve effect has been greatly reduced in the logic region 204 of the embedded memory 200. Thus, processing of the embedded memory 200 is facilitated.

A method and system has been disclosed for using a plasma etch, which an ARC layer is resistant to, in order to remove a photoresist structure. Thus, the ARC layer is preserved for subsequent use. Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A method providing a semiconductor device, the semiconductor including a first layer desired to be etched, the method comprising the steps of:

(a) providing an antireflective coating (ARC) layer having antireflective properties;

(b) patterning a resist layer, the resist layer including a pattern having a plurality of apertures therein for etching the first layer, a first portion of the first layer and a second portion of the ARC layer being exposed by the pattern;

(c) etching the first portion of the first layer and the second portion of the ARC layer; and

(d) removing the resist layer utilizing a plasma etch, the ARC layer being resistant to the plasma etch.

2. The method of claim 1 wherein the ARC layer providing step (a) further includes the steps of:

(a1) depositing the ARC layer.

3. The method of claim 1 wherein the ARC layer further includes an SiON layer and wherein the resist layer removing step (d) further includes the step of:

(d1) performing the plasma etch using a plasma including a forming gas, the ARC layer being resistant to the plasma etch using the plasma including the forming gas.

4. The method of claim 3 wherein the plasma further includes four percent of the forming gas.

5. The method of claim 3 further comprising the step of:

(e) providing a wet preclean after the plasma etching step (d).

6. The method of claim 1 wherein the ARC layer is a SiON ARC layer and wherein a thickness of the SiON ARC layer is three hundred Angstroms plus or minus no more than approximately ten percent.

7. A semiconductor device comprising:

a plurality of memory cells including a plurality of stacked gates; and

wherein the plurality of stacked gates are provided using an antireflective coating (ARC) layer that is resistant to removal by a plasma etch, a portion of the semiconductor device is provided using a resist layer, the resist layer being removed using the plasma etch.

8. The semiconductor device of claim 7 wherein the ARC layer further includes an SiON layer and wherein the resist layer is removed using by the plasma etch which uses a plasma including a forming gas, the ARC layer being resistant to the plasma etch using the plasma including the forming gas.

9. The semiconductor device of claim 8 wherein the plasma further includes four percent of the forming gas.

10. The semiconductor device of claim 7 wherein the ARC layer is a SiON ARC layer and wherein a thickness of the SiON ARC layer is three hundred Angstroms plus or minus no more than approximately ten percent.

11. The semiconductor device of claim 7 further comprising:

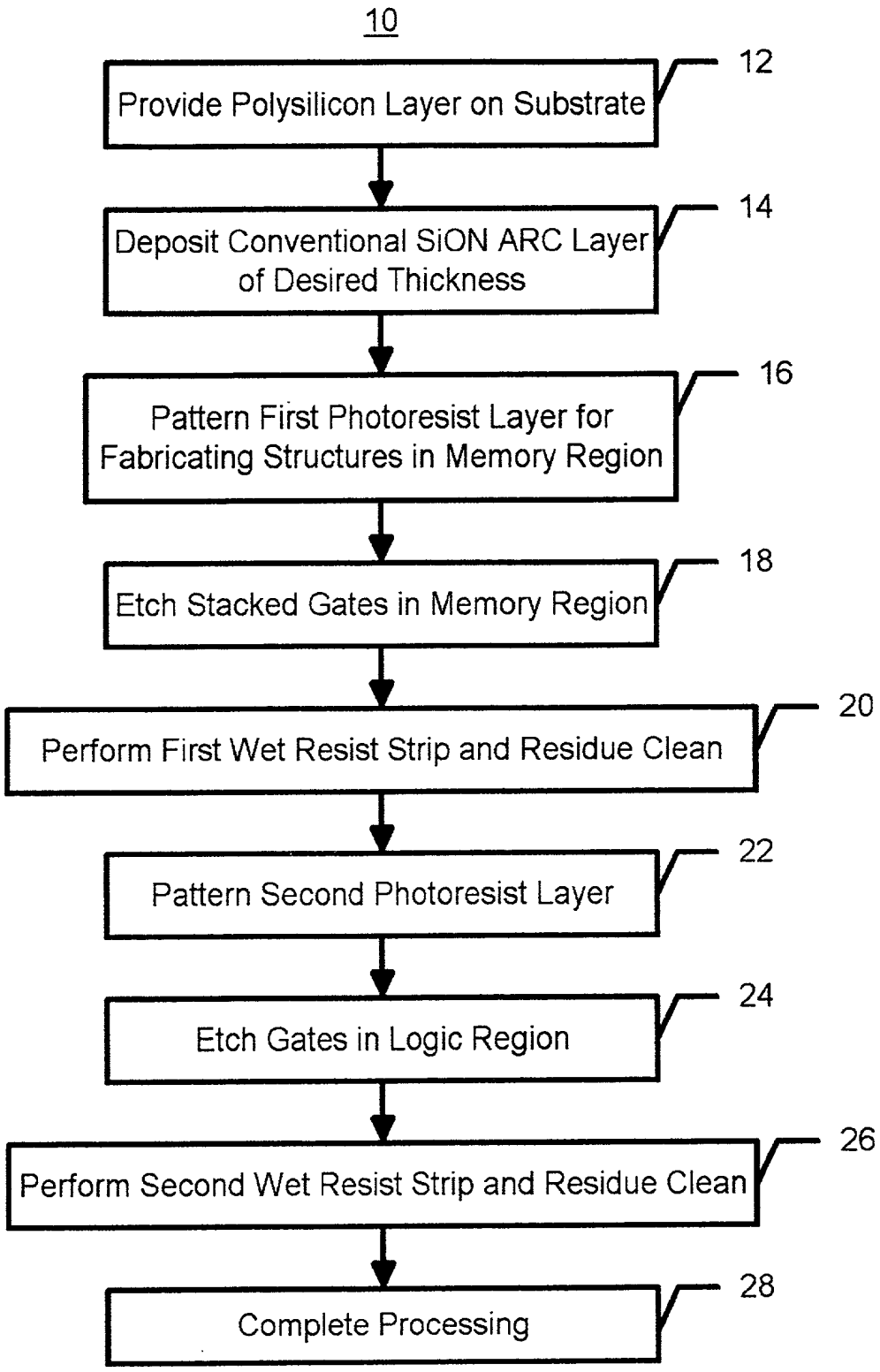
a plurality of logic cells;

wherein the plurality of logic cells are defined using the ARC layer that is resistant to removal by the plasma etch.

12. The semiconductor device of claim 11 wherein a portion of the semiconductor device provided using the resist layer includes the plurality of memory cells.

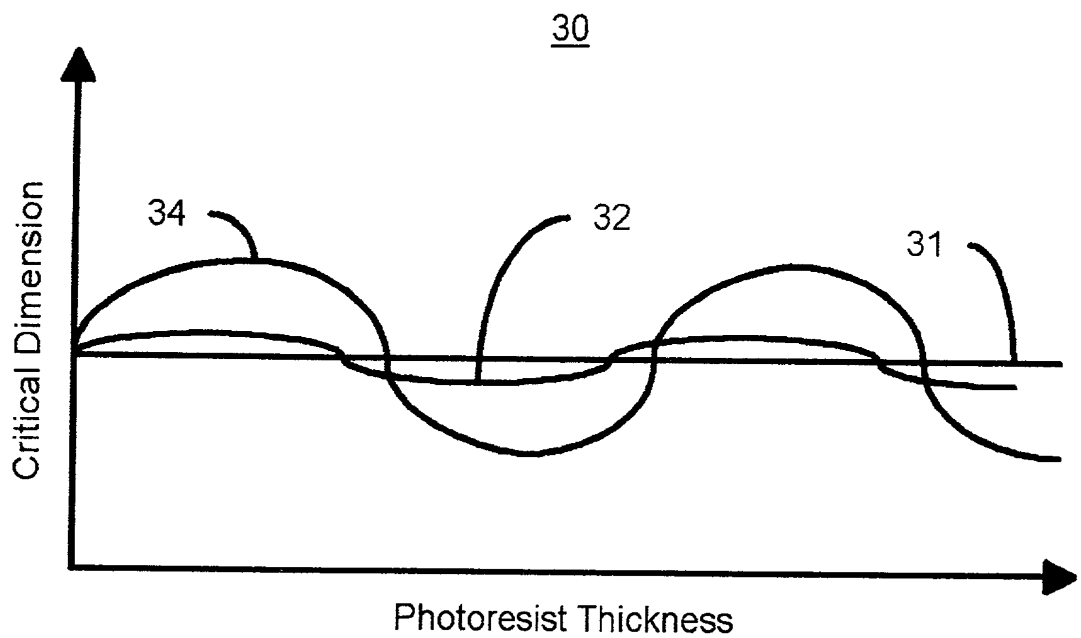
ABSTRACT

A method and system for providing a semiconductor device is disclosed. The semiconductor device includes a first layer to be etched. The method and system include depositing an antireflective coating (ARC). At least a portion of the ARC layer is on the first layer. The method and system also include patterning a resist layer. The resist layer includes a pattern having a plurality of apertures therein. The resist layer is for etching the first layer. A first portion of the first layer and a second portion of the ARC layer are exposed by the pattern. The method and system also include etching the first portion of the first layer and the second portion of the ARC layer and removing the resist layer utilizing a plasma etch. The ARC layer is resistant to the plasma etch.



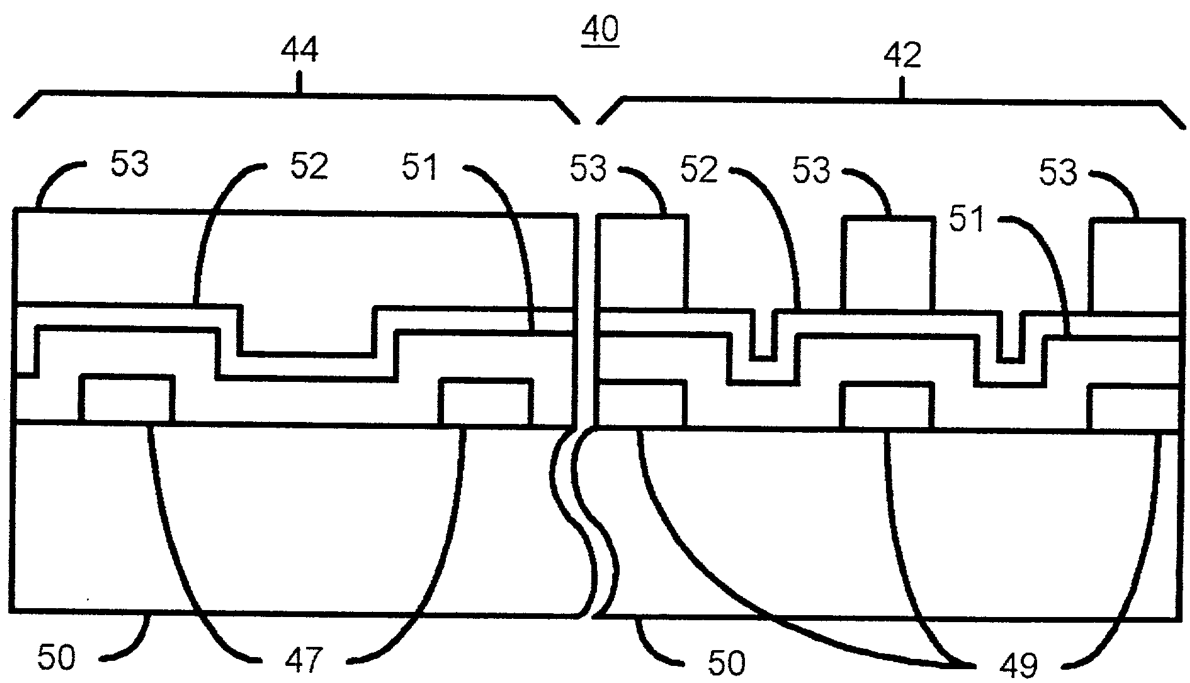
Prior Art

Figure 1



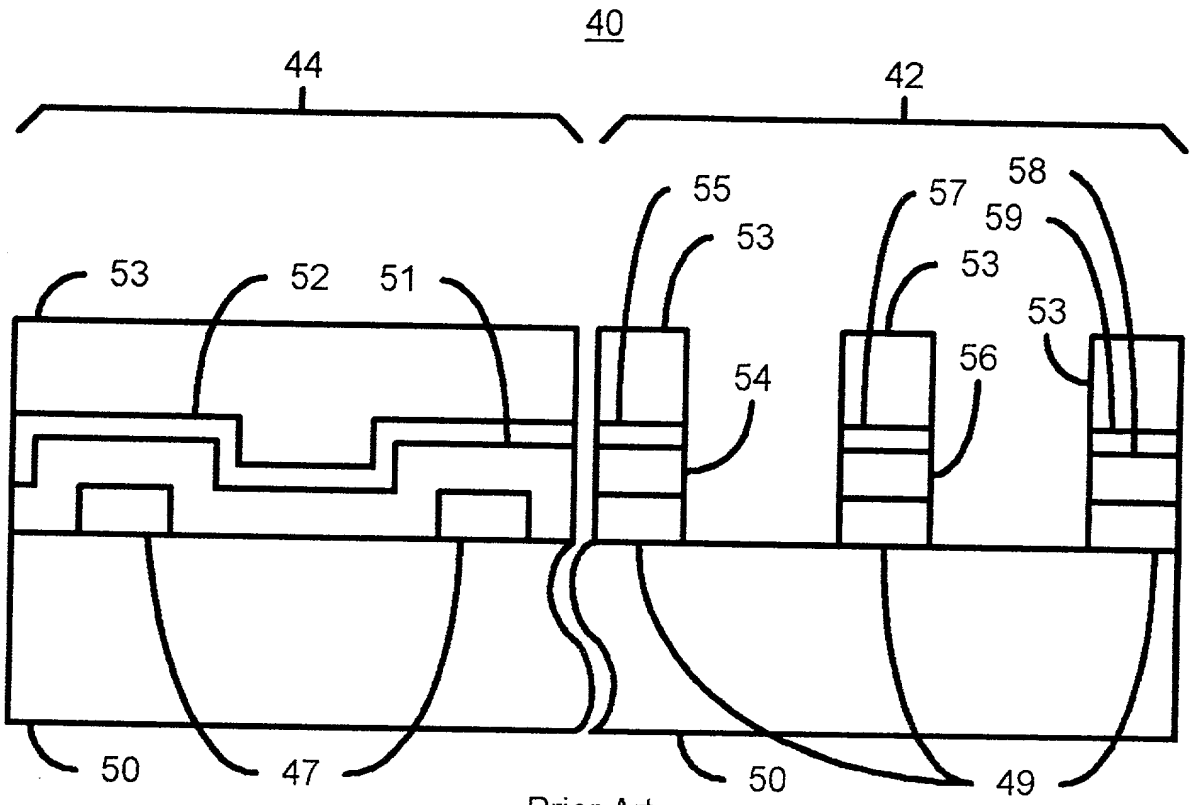
Prior Art

Figure 2



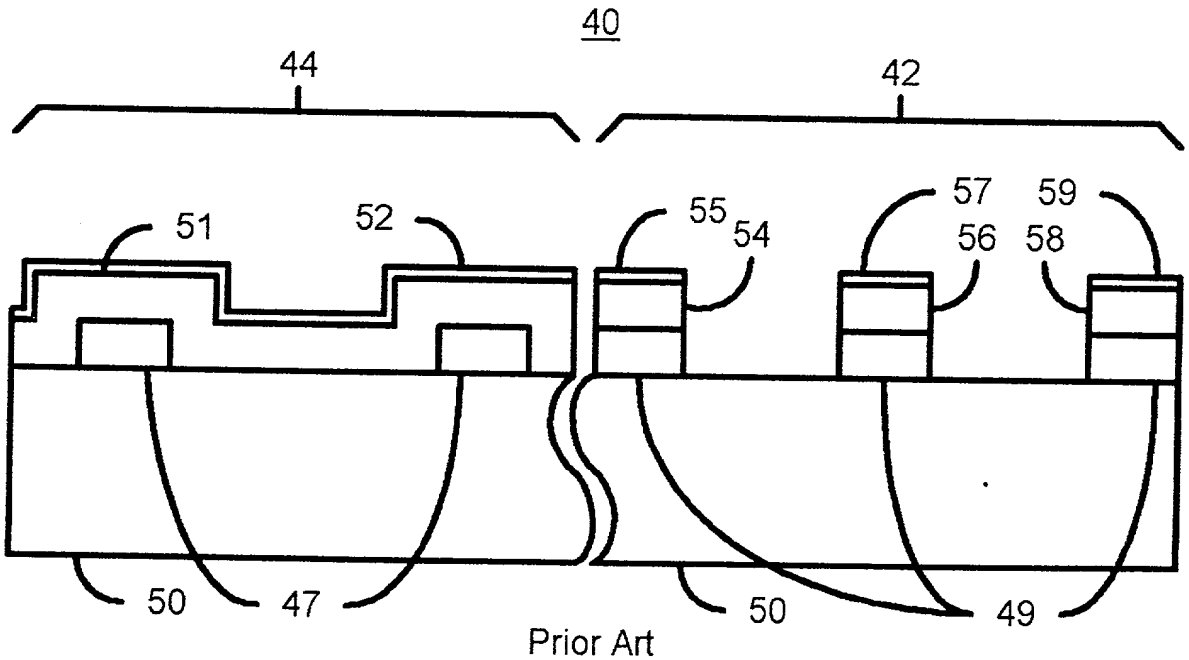
Prior Art

Figure 3A



Prior Art

Figure 3B



Prior Art

Figure 3C

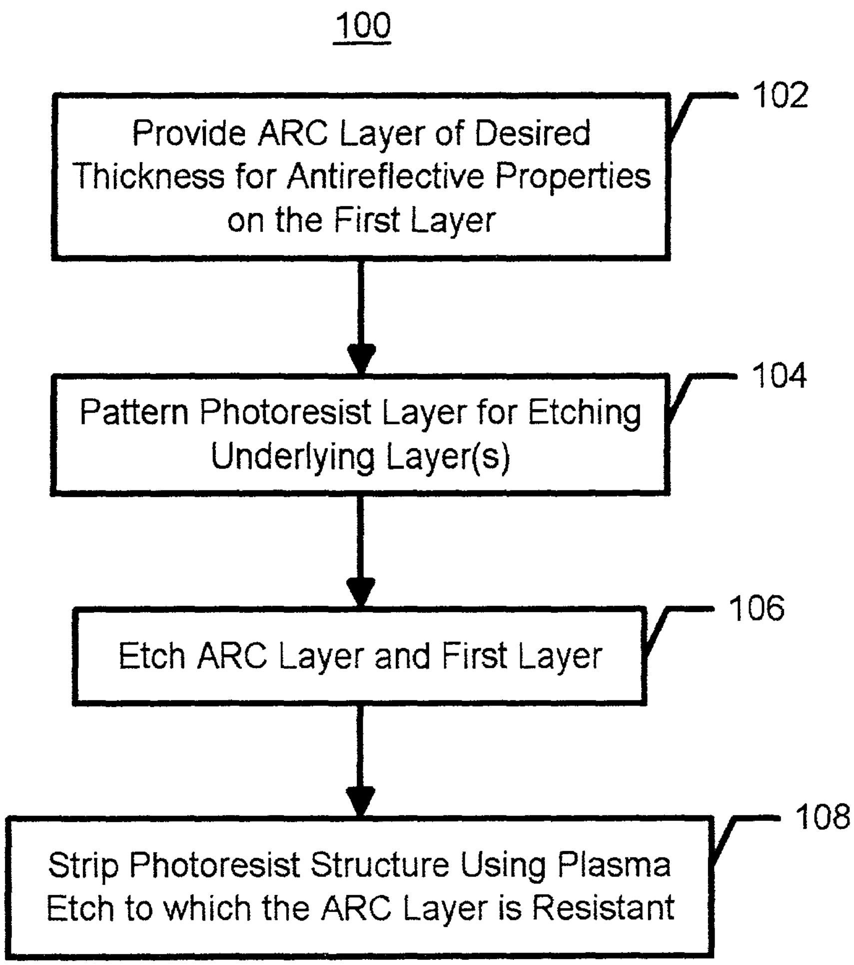

100
Provide ARC Layer of Desired Thickness for Antireflective Properties on the First Layer
102
Pattern Photoresist Layer for Etching Underlying Layer(s)
104
Etch ARC Layer and First Layer
106
Strip Photoresist Structure Using Plasma Etch to which the ARC Layer is Resistant
108

Figure 4A

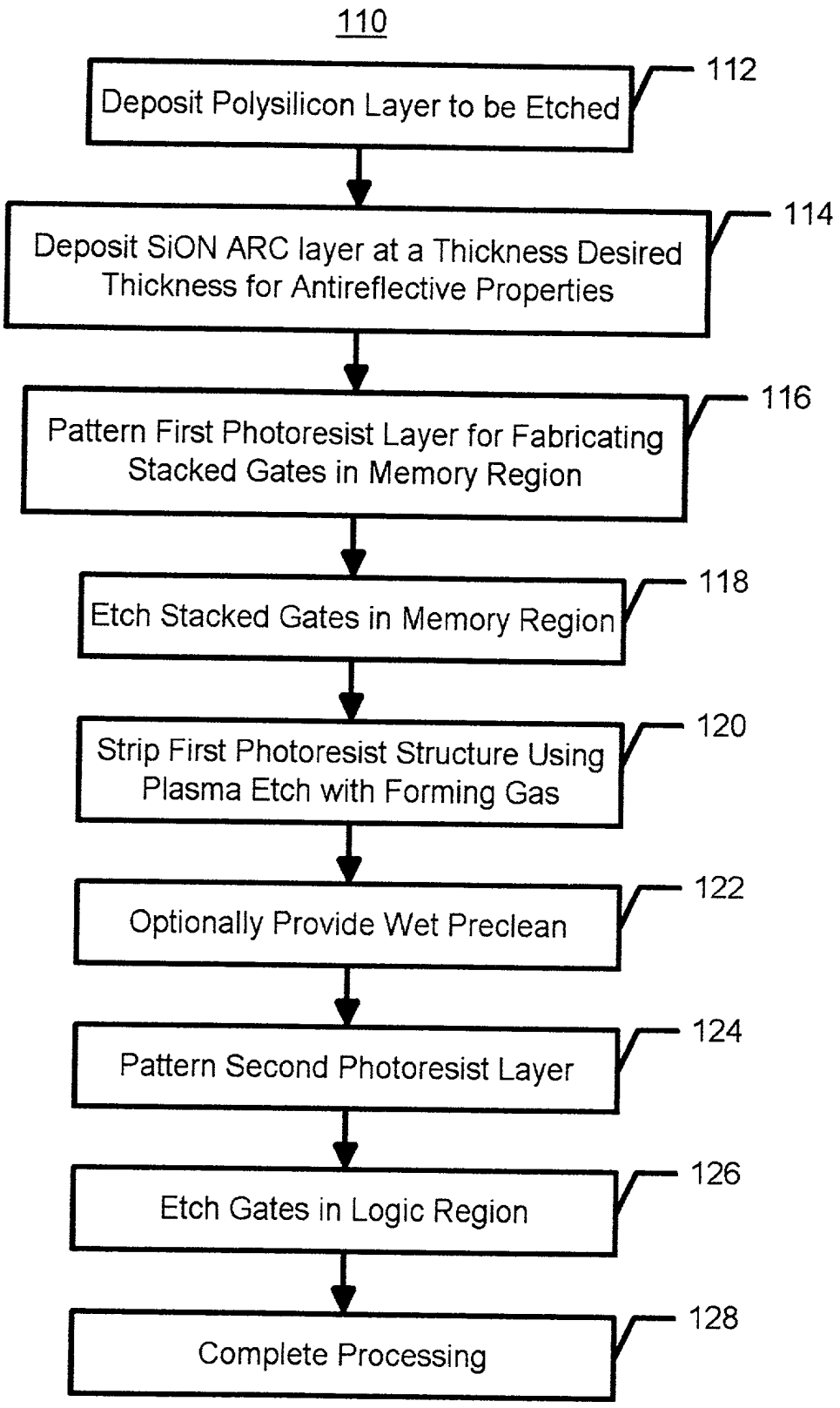

110
Deposit Polysilicon Layer to be Etched
112
Deposit SiON ARC layer at a Thickness Desired Thickness for Antireflective Properties
114
Pattern First Photoresist Layer for Fabricating Stacked Gates in Memory Region
116
Etch Stacked Gates in Memory Region
118
Strip First Photoresist Structure Using Plasma Etch with Forming Gas
120
Optionally Provide Wet Preclean
122
Pattern Second Photoresist Layer
124
Etch Gates in Logic Region
126
Complete Processing
128

Figure 4B

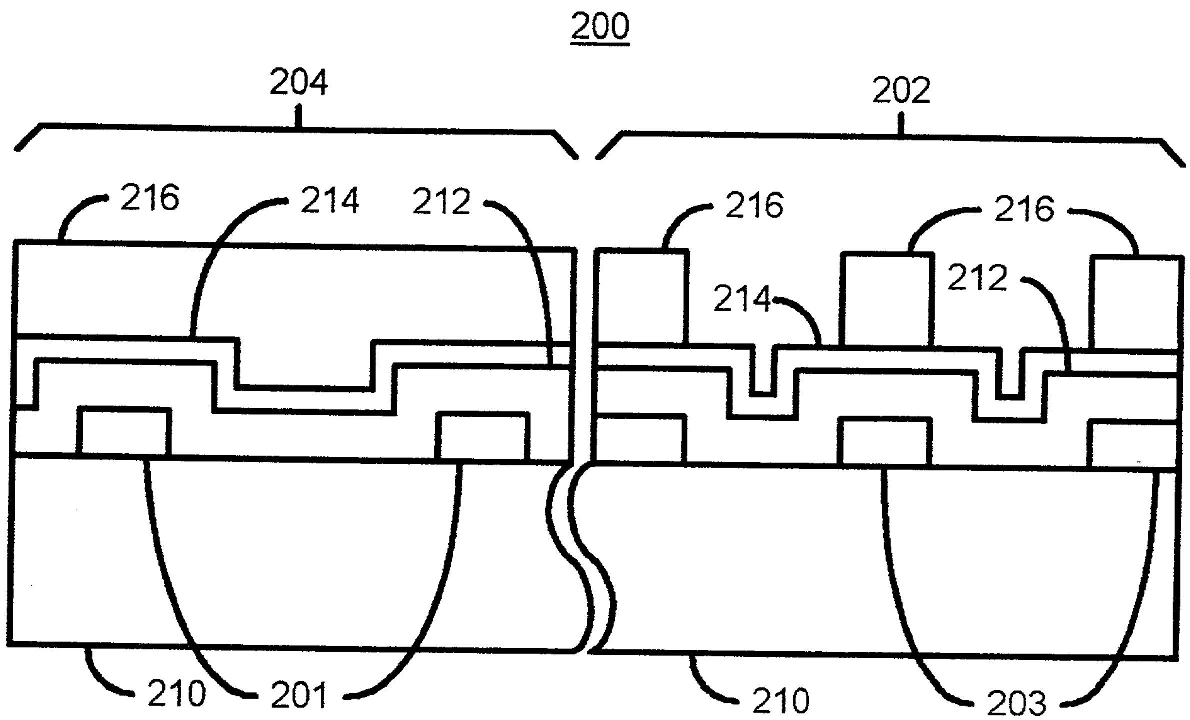


Figure 5A

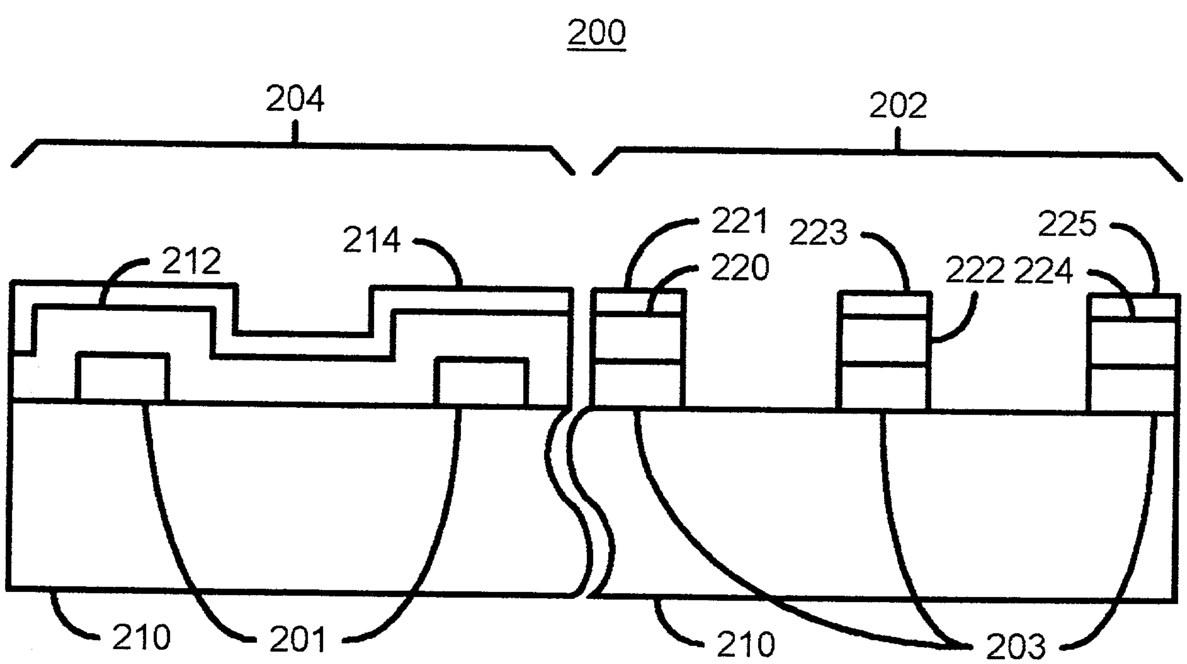


Figure 5B

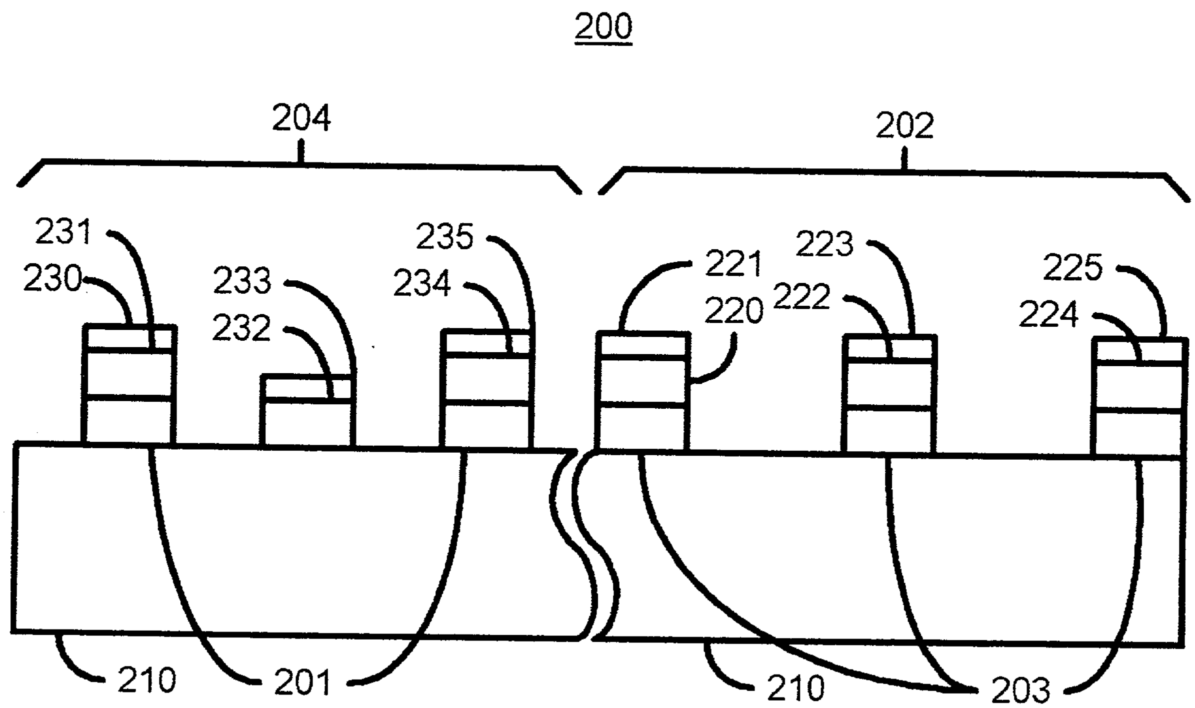

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Figure 5C

COPY

DECLARATION

As the below named join-inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe I am the first, original and joint-inventor of the invention entitled:

METHOD AND SYSTEM FOR REDUCING ARC LAYER REMOVAL DURING REMOVAL OF PHOTORESIST

described and claimed in the specification which is attached hereto that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; that I do not know and do not believe the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, that I acknowledge my duty to disclose information of which I am aware that is material to the examination of this application as defined by 37 C.F.R. ∋1.56, and that no application for patent or inventor's certificate on said invention has been filed in any country foreign to the United States of America by my or by my legal representatives or assigns.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Date

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Signature of Inventor

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Date

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